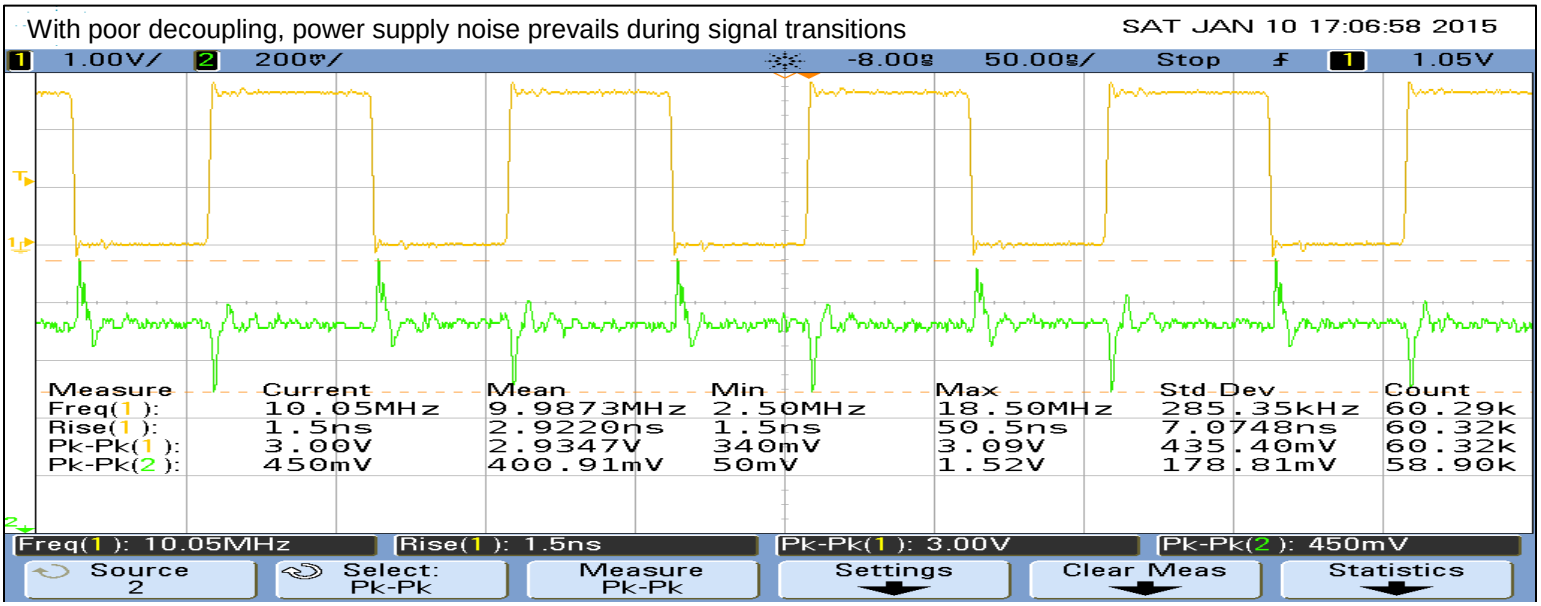
Practical Power Integrity Applications
3-Day Practical Training



Power Integrity & High-Speed PCB Design

With the advancement of today's technology, high-speed devices have rise/fall times in sub-ns. The fast slew rate can contribute to signal integrity (SI) and power integrity (PI) problems, such as signal reflection, crosstalk, simultaneous switching noise (SSN) and ground bounce. As far as PI is concerned, frequency response of decoupling capacitors, interconnect parasitic inductance and impedance profile of a power distribution system will influence the stability of power supply in high-speed PCBs. Failure to design a stable power supply system in a PCB may result in impaired signals, jitter problem and violation of EMC regulations.

About Go Training

Go Training applies effective pedagogical methodologies that demonstrate case studies and hands-on practical skills, in addition to explaining clearly how things work in principle. Every course that we conduct is delivered by a subject matter expert who holds the academic qualification and working experience in that specialization. On the days when they are not teaching, our trainers work on consultancy projects and technical deliveries. Their work has received numerous recognition and awards in the industry. Our team of trainers has been invited as keynote speakers at numerous international conferences, and as principal consultants for various industries.

Date: 17-19August 2015
(Monday - Wednesday)
Time: 0900 - 1700
Venue: Suite 2B-21-1, Level 21, Block 2B, Plaza Sentral, Jalan Stesen Sentral 5, KL Sentral, 50470 Kuala Lumpur, Malaysia.

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Course Outline

Day 1:

Introduction to Power Integrity:
- Power supply system in a PCB
- Noise in power supply and consequences
- Challenges on power supply in high-speed PCBs
- Purposes of power decoupling
- Basic design rules for achieving a stable power supply
- Transient power supply currents in ICs

Capacitors
- ESR, ESL and self-resonant frequency of capacitors
- Package size versus ESL
- ESL and capacitor performance
- Types of capacitors - bulk, decoupling, planar
- Effective planar capacitance area

Mounting Inductance of Capacitors
- Capacitor trace inductance
- Via pair loop inductance
- Spreading inductance
- PCB stack-up configuration versus power supply inductance
- When location of capacitor matters
- IC package inductance

Power Integrity Analysis
- DC drop analysis
- AC noise analysis
- Decoupling analysis
- Power plane resonance
- Voltage fluctuation, transient current and target impedance

Hands-on Session: Demonstrating PI issues via simulation/measurement

Day 2:

Impedance Profile of a Power Distribution Network
- What is power distribution network (PDN)
- Impedance profile of a PDN
- Anti-resonance n parallel connected capacitors
- How to reduce anti-resonance peak
- Number of capacitors needed for a PDN
- Capacitors - use same or different values
- Interaction between decoupling and planar capacitors

Ground bounce and Simultaneous Switching Noise
- Mechanism of ground bounce and SSN
- How ground bounce causes logic errors
- How SSN couples to signals
- Method for reducing ground bounce and SSN

Hands-on Session: Demonstrating PI issues via simulation/measurement

Day 3:

Practical Layout Techniques for Achieving Good Power Integrity
- Power entry filter layout techniques
- DC-DC converter layout techniques
- PCB stack-up configurations that provide good power decoupling
- Mounting techniques that minimize capacitor inductance
- Decoupling capacitors placement on high-current termination islands
- Minimizing loop area by proper arrangement on power and ground vias
- Why differential signaling is immune to common-impedance coupling
- Isolation between noisy and quiet ground islands
- Decoupling capacitors and return current design

Hands-on Session: Demonstrating PI issues via PCB Layout Design

About the Instructor

Mr Chai Ched Chang received his B.Eng (Hons) from University of Malaya, and M.EngSc from Multimedia University, Malaysia. Mr Chai began his career as a Signal Integrity engineer in 2001, specialized in designing High-Speed PCB.

He had delivered many consumer electronics PCB designs, where he is specifically experienced in resolving SI issues associated with high-speed memory (SDRAM, DDR, DDR2, DDR3), differential signaling (LVDS, HDMI, USB, PCI Express, Ethernet), and other digital interfaces (FPGA interface, FLASH memory, Video bus, ADC & DAC). He also has vast experience in making PCB stack-up, high-speed signal simulation and analysis.

In 2012, Mr Chai left his former company as Chief Technical Officer, and started iRtec Consulting Sdn Bhd. He also practices as a trainer since then and has shared his experience with over 400 engineers. With over two decades of combined experience in both research and industry, he continues to strive to provide the best consultation services to his clients.

Go Training
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