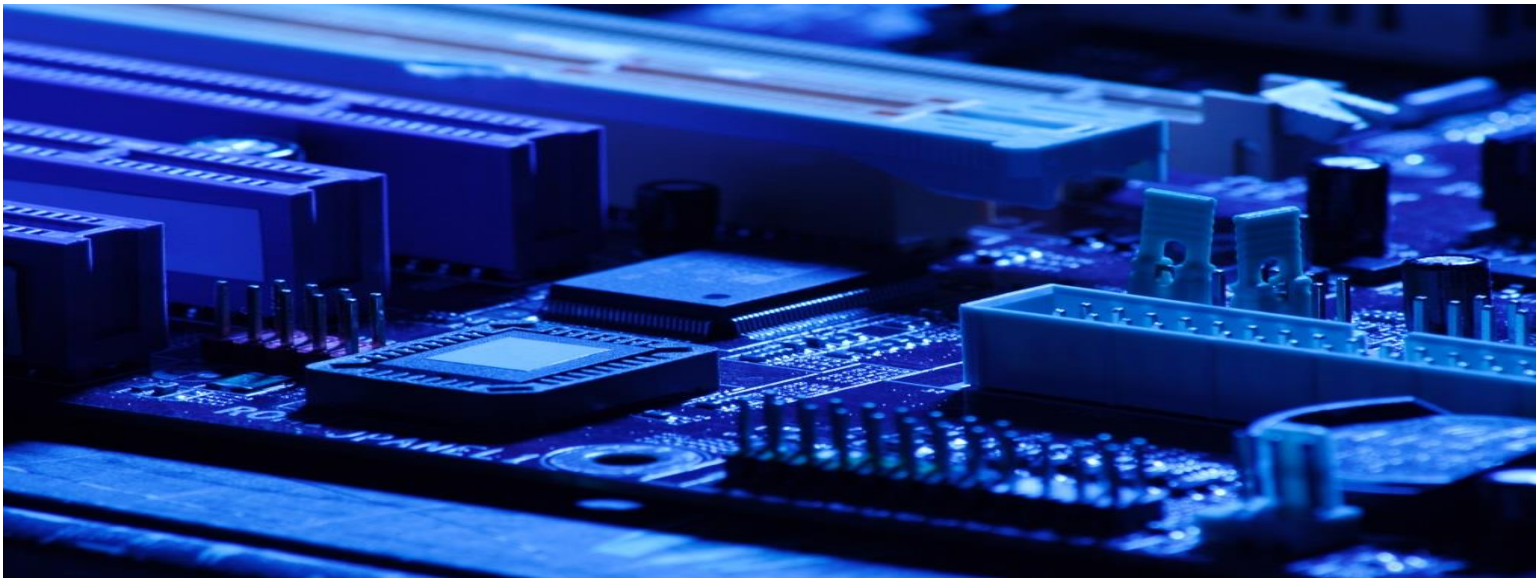
Practical Signal Integrity Applications

3-Day Key Concepts, Real-life Examples and Handy Guidelines



Signal Integrity & High-Speed PCB Design

With the advancement of today's technology, high-speed devices have rise/fall times as low as 1 ns. Signal traces in the printed circuit board (PCB) can no longer be treated as simple short-circuit interconnects; instead they behave as transmission lines. The fast slew rate can contribute to signal integrity (SI) and electromagnetic interference (EMI) problems, such as impedance mismatch, signal reflection, crosstalk, ground bounce and radiation. Thus, it is highly possible that a high-speed PCB fails to work due to SI & EMI issues. Proper PCB design techniques and good understanding of high-speed concepts are required to ensure the smooth transition from circuit design to first prototype and final product.

About Go Training

Go Training applies effective pedagogical methodologies that demonstrate case studies and hands-on practical skills, in addition to explaining clearly how things work in principle. Every course that we conduct is delivered by a subject matter expert who holds the academic qualification and working experience in that specialization. On the days when they are not teaching, our trainers work on consultancy projects and technical deliveries. Their work has received numerous recognition and awards in the industry. Our team of trainers has been invited as keynote speakers at numerous international conferences, and as principal consultants for various industries.

Date: 18-20 May 2015
(Monday - Wednesday)
Time: 0900 - 1700
Venue: Suite 2B-21-1, Level 21, Block 2B, Plaza Sentral, Jalan Stesen Sentral 5, KL Sentral, 50470 Kuala Lumpur, Malaysia.

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Course Outline

Day 1

Introduction to Signal Integrity
- What are SI, EMI, EMC and High-Speed PCB
- What are the common problems in High-Speed PCB

Transmission Lines and Signal Propagation
- Lumped versus distributed circuit
- What are transmission lines and critical length
- Effects of signal reflections to digital circuitry functionality and timing
- Transmission lines termination schemes (Series, Parallel, RC, etc)
- Discontinuities in transmission lines
- Periodic pulses and knee frequency
- Attenuation and dispersion
- Layout techniques for transmission lines

Signal Return Path and EMI
- How does high-speed signal return to its source
- Perforation and splits in reference plane
- Common mode currents
- Layout techniques for minimizing EMI

Hands-on Session: Demonstrating SI issues via simulation/measurement

Day 2

PCB Stack-up
- What factors to consider when making a PCB stack-up
- How to control trace impedance (Zo) for microstrip and stripline
- Criteria of a PCB stack-up configuration that promote good SI
- Steps in making a PCB stack-up

SSN – Ground Bounce
- What causes ground bounce
- Effect of ground bounce on driver/receivers voltage levels
- How to minimize ground bounce problem

Decoupling Capacitors
- Functions of bypass capacitors
- Effects of ESL on capacitors
- Package vs inductance
- Placement and layout techniques that minimize loop inductance
- Power Distribution Network

Hands-on Session: SI case study

Day 3

Crosstalk
- What causes crosstalk and the effects on signal
- Factors that affect near-end and far-end crosstalk
- Crosstalk on microstrip vs stripline
- What factors can be controlled for minimizing crosstalk
- Layout techniques for minimizing crosstalk

Differential Signaling
- The importance of differential signaling
- EMI issues on differential signaling
- Which is better: tightly coupled or loosely coupled lines
- How to select suitable W/S for controlling differential impedance (Zdiff)
- Layout techniques for differential pairs

Quality high-speed PCB Design Procedure
- Steps in designing high-speed boards
- What analysis is required
- Useful rules for achieving good SI
- Timing skew adjustment
- Case study

Hands-on Session: Demonstrating SI issues via simulation/measurement

About the Instructor

Mr Chai Ched Chang received his B.Eng (Hons) from University of Malaya, and M.EngSc from Multimedia University, Malaysia. Mr Chai began his career as a Signal Integrity engineer in 2001, specialized in designing High-Speed PCB. He had delivered many consumer electronics PCB designs, where he is specifically experienced in resolving SI issues associated with high-speed memory (SDRAM, DDR, DDR2, DDR3), differential signaling (LVDS, HDMI, USB, PCI Express, Ethernet), and other digital interfaces (FPGA interface, FLASH memory, Video bus, ADC & DAC). He also has vast experience in making PCB stack-up, high-speed signal simulation and analysis. In 2012, Mr Chai left his former company as Chief Technical Officer, and started his own company, iRtec Consulting Sdn Bhd. With 15 years of combined experience in both research and industry, he continues to strive to provide the best Signal Integrity consultation service to his clients.

Go Training
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