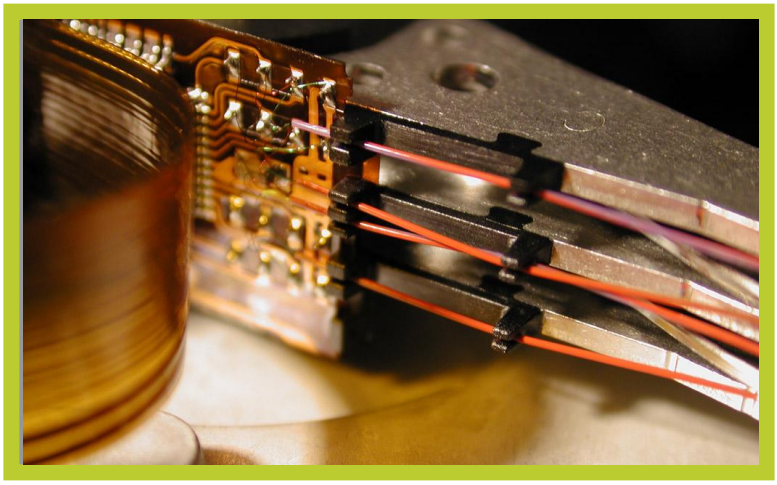
3-Day Practical Real-Time DSP using FPGA

Real-Time DSP using FPGA

Traditionally, digital signal processing (DSP) algorithms are implemented on specialized programmable processors, which are inherently sequential, with fixed arithmetic capabilities, and hence have lower performance than the field programmable gate arrays (FPGAs). In order to satisfy real-time and high precision requirements, many of today's front-end DSP algorithms have been implemented using FPGA. This course covers the core DSP algorithms in filtering, frequency analysis and signal generation. Hands-on sessions will be provided to illustrate a complete end-to-end design flow of a FPGA-based real-time DSP.



Course Outline

Day 1
Review of DSP Concepts
- What is signal
- What are the key elements of a DSP system
- How to perform frequency domain analysis
- What is an FIR filter, how to construct FIR filter structures

DSP on FPGA
- What are the available DSP implementation platforms
- What is FPGA, current trends
- Why DSP on FPGA
- Overview of FPGA-based DSP system design flow

Hands-on Session 1-1: Basics of Matlab/Scilab

Hands-on Session 1-2: Practical implementation of real-time DSP on FPGA

Day 2
Essentials of DSP Arithmetic
- What is 2's complement number system
- What is fixed point arithmetic
- Fixed point versus floating point DSPs
- How to deal with the word-length issues

Verilog HDL for DSP
- How to model digital circuit with Verilog
- How to verify a Verilog model with testbench
- How to build basic DSP arithmetic blocks
- How to implement fixed point arithmetic with Verilog
- Enhanced DSP features using FPGAs

Hands-on Session 2-1: Fixed-point FIR filtering using Matlab/Scilab

Hands-on Session 2-2: Real-time digital filtering on FPGA

Day 3
Fast Fourier Transform (FFT)
- What is FFT
- Overview of various FFT algorithms
- How to design an N-point radix-2 FFT
- How to implement N-point radix-2 FFT with Verilog

Direct Digital Synthesizer (DDS)
- What is DDS, its advantages over memory-based approach
- How to implement DDS with Verilog
- How to design a single-tone signal synthesizer
- How to design an arbitrary waveform generator

Hands-on Session 3-1: Spectrum analysis and matched filtering

Hands-on Session 3-2: Designing a FPGA-based digital frequency synthesizer

GO TRAINING

Public Training Session
Open for Registration

"Lots of examples"
"Very practical course"
"Useful tips for real-time DSP"
"I managed to create a FPGA-based DSP in just 3 days!"

Date: 26 - 28 September 2012 (Wed - Fri)

Time: 0900 - 1700

Venue: Details as follows

Redang Ballroom, 1st Floor, Main Club House
Bukit Jalil Golf & Country Resort
Jalan Jalil Perkasa 3, Bukit Jalil
57000 Kuala Lumpur, Malaysia

Register by 7 September 2012 to enjoy early bird discount.
Certificate will be awarded to participants who complete the training.
Lunch, refreshments and training handout provided and included.
Transportation and accommodation not included.

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About Go Training

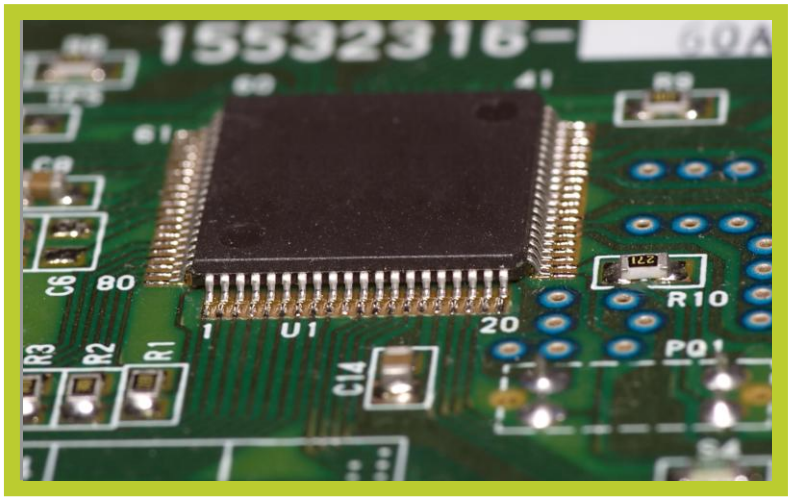
Go Training applies effective pedagogical methodologies that demonstrate case studies and hands-on practical skills, in addition to explaining clearly how things work in principle. Every course that we conduct is delivered by a subject matter expert who holds the academic qualification and working experience in that specialization. On the days when they are not teaching, our trainers work on consultancy projects and technical deliveries. Their work has received numerous recognition and awards in the industry. Our team of trainers has collectively published more than 100 international journal and conference papers, and 2 technical text books. Some have also been invited as keynote speakers at numerous international conferences, and as principal consultants for various industries.

About the Instructor

Mr Ng Mow Song received his B.Eng (Hons) in Electrical Engineering from University of Malaya, Malayisa, and M.EngSc from Multimedia University, Malaysia. He began his academic career as a tutor at the Faculty of Engineering, Multimedia University in 1998, was later promoted to be a lecturer, and then moved on to Universiti Tunku Abdul Rahman in 2008. His expertise is digital signal processing, embedded system design, ASIC design methodology, and VLSI modeling and verification.

Since 2006, Mr Ng has been working on hardware accelerator design of the discrete wavelet transform, smart video surveillance system, and digital audio analysis algorithms with industrial partners. He was a visiting lecturer in Agilent Technologies, Malaysia from 2007 to 2009 to work on signal processing algorithm. He is currently working on a multicore System-on-Chip IC design project with another industrial partner.

Over the years, Mr Ng has been conducting regular training sessions on digital signal processing and FPGA design. His most regular participants are hardware and software designers from multinational electronics manufacturers in Malaysia, and occasionally researchers from MIMOS, lecturers from RMUTT, Thailand and PSDC experienced engineers. He has also delivered numerous 3-week long job camps for university graduates to enhance their DSP knowledge and hardware programming skill.



Hands-on session: FPGA-based DSP implementation

HANDS ON LEARNING WITH LATEST TECHNOLOGY

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Technical Training by Expert in the Field

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